11-21-00

A

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael R. May et al.

Docket No. SIG000050

Title: A METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

Date: ~~11-13-2000~~ 11/20/00

To the Honorable Commissioner
of Patents and Trademarks
Box Patent Application
Washington, D.C. 20231

REQUEST FOR FILING A NATIONAL PATENT APPLICATION

The applicants respectfully request that the above captioned patent application be accepted for examination. This patent application is a:

- [X] new patent application
- [ ] continuation in part (CIP) of Application Serial No. [ ] filed on [ ]
- [ ] divisional application of Application Serial No. [ ] filed on [ ]
- [ ] continuation application of Application Serial No. [ ] filed on [ ]

Accompanying this request is (as indicated by an "X" in the corresponding box):

- [X] 1. 16 pages of specification, which includes the claims and abstract, and 4 sheets of formal drawings;
- [X] 2. Combined Declaration and Power of Attorney;
- [ ] 3. An Information Disclosure Statement along with the references;
- [ ] 4. A petition to extend the response for a priority application identified above;
- [X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;
- [X] 6. An assignment recording cover sheet;
- [X] 7. A verified statement establishing small entity status under 37 C.F.R Sections 1.9 and 1.27;
- [X] 8. A certificate of mailing indicating that the above captioned patent application has been deposited as "Express Mail" with the United States Postal Service;
- [ ] 9. A certificate of mailing indicating that the above captioned patent application has been deposited with the United States Postal Service with sufficient postage as first class mail;
- [X] 10. A return postcard; and
- [ ] 11. A preliminary amendment.

The filing fee for the above captioned patent application is as follows:

Large entity status apply? no

				basic filing fee	355.00
total claims	22	extra per claim fee	9.00	extra claim fee	18.00
total ind claims	3	extra per ind claim fee	40.00	extra ind claim fee	0.00
				assign record fee	40.00
				TOTAL FILING FEE	413.00

Payment of the above calculated filing fee is as follows (as indicated by the "X" in the corresponding box):

[ ] A check in the amount of $

[X] Please charge Deposit Account No. 501415 in the amount of $ 413.00
A duplicate sheet is attached.

Respectfully submitted,

By: ____________________

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SIG000050

Customer No: 000024263
SigmaTel, Inc.,
2700 Via Fortuna, Suite 500
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael R. May et al. Examiner:

Serial No. Art Group:

Filing Date: Docket No. SIG000050

Title: A METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

~~11/13/~~2000
11/20/00

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

CERTIFICATE OF EXPRESS MAILING

Express Mail Lab EL581297982US Name of Depositor: Diane Hudson

Date of Deposit: 11-20-00 Signature: Diane Hudson

I hereby certify that this paper and the items identified below are being deposited with the U.S. Postal Service "Express Mail Post Office to Addresses" service under 37 C.F.R. Section 1.10 on the 'Date of Deposit', indicated above, and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Items accompanying this Certificate of Express Mailing:

- [X] 1. A new patent application including 16 pages of specification, and 4 sheets of formal drawings;
- [X] 2. Combined Declaration and Power of Attorney;
- [ ] 3. An Information Disclosure Statement along with the references;
- [ ] 4. A petition to extend the response for a priority application identified above;
- [X] 5. An assignment assigning all rights in the above referenced patent application to SigmaTel, Inc.;
- [X] 6. An assignment recording cover sheet;
- [X] 7. A verified statement establishing small entity status under 37 C.F.R. Sections 1.9 and 1.27;
- [X] 8. A return postcard; and
- [ ] 9. A preliminary amendment.

SigmaTel, Inc.
Customer No: 000024263

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael R. May et al.	Examiner:	
Serial No.		Art Group:	
Filing Date:		Docket No.	SIG000050

Title: A METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

11/~~13/20~~00
11/20/00

To the Honorable Commissioner
of Patents and Trademarks
Washington, D.C. 20231

STATEMENT OF STATUS AS SMALL ENTITY
Pursuant to 37 C.F.R. Section 1.27 and Section 1.9

For the above captioned patent application, a party in interest avers that it qualifies for small entity status as SMALL BUSINESS CONCERN. To verify the small entity status, the party in interest attests that:

1. This verified statement for the above captioned patent application or patent is being submitted prior to or with the first fee paid as a small entity;

2. For purposes of this verified statement, as defined in 37 C.F.R. Section 1.27, a license to a Federal agency resulting from a funding agreement with that agency pursuant to 35 U.S.C. 202 (c) (4) does not constitute a license.

3. As a SMALL BUSINESS CONCERN:
(a) I swear that I am an official of SigmaTel, Inc., empowered to act on behalf of SigmaTel, Inc.,
(b) In my capacity as identified in this section 3(a), I swear that SigmaTel, Inc. qualifies as a small business concern as defined in 37 C.F.R Section 1.9 and that the number of employees of SigmaTel, Inc. and those of its affiliates, does not exceed 500 persons;
(c) I further swear that my signature appears at the end of this Statement of Status as Small Entity;
(d) I still further swear that, in support my of contention that SigmaTel, Inc. qualifies as a small business concern, exclusive rights to the invention of the above captioned patent application have been conveyed to and remain with SigmaTel, Inc.,

Signatures of Person(s) Making the Verified Statement

SigmaTel, Inc. (Customer No:000024263)
Name: Timothy W. Markison

[signature]
Signature
Title: General Counsel

Date 11/29/00

PATENT APPLICATION

SIG000050

METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to integrated circuits and more particularly to enabling a stand-alone integrated circuit.

BACKGROUND OF THE INVENTION

Integrated circuits are known to include a large amount of circuitry in a very small area. The circuitry may perform a wide variety of functions such as a microprocessor, digital signal processor, operational amplifier, integrator, audio encoder, audio decoder, video encoder, video decoder, et cetera. To power such integrated circuits, the integrated circuits include power pins for a power input (typically V_{dd}) and a return pin (typically V_{ss}). The power is typically provided by a regulated external power supply. As such, once the external power supply is up and running, the integrated circuit may be activated in a known state.

For most digital circuits on an integrated circuit, a clock signal is needed. The clock is typically generated once an external power supply is producing a regulated supply voltage to the integrated circuit (IC) and the IC has been activated. To ensure that the digital circuitry begins functioning in a known state, it is important to delay activation of the digital circuit until the power supply is producing a stable supply voltage and the clock is operating properly. Once these operating parameters are ensured, the digital circuitry may be activated.

Insuring the proper enablement of an IC is relatively straightforward when the power supply is external to the IC. If, however, the power converter is on-chip with the digital circuitry and the power converter requires a clock signal to produce a supply voltage, a difficulty arises in enabling such a stand-alone integrated circuit.

Therefore, a need exists for a method and apparatus for enabling a stand-alone integrated circuit that includes an on-chip power converter.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic block diagram of a stand-alone integrated circuit in accordance with the present invention;

Figure 2 illustrates a schematic block diagram of an alternate stand-alone integrated circuit in accordance with the present invention;

Figure 3 illustrates a logic diagram of a method for enabling a stand-alone integrated circuit in accordance with the present invention; and

Figure 4 illustrates a schematic block diagram of an embodiment of the reset circuit of Figure 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Generally, the present invention provides a method and apparatus for enabling a stand-alone integrated circuit (IC). Such a method and apparatus includes processing that begins by establishing an idle state that holds at least a portion of the stand-alone integrated circuit in a reset condition when a power source is operably coupled to the stand-alone integrated circuit. A stand-alone integrated circuit includes generally an on-chip power converter, a reset circuit and some functional circuitry which may be a

microprocessor, digital signal processor, digital circuitry, state machine, logic circuitry, analog circuitry, and/or any type of components and/or circuits that perform a desired electrical function. When a power enable signal is received, the on-chip power converter is enabled to generate at least 1 supply (e.g. a voltage supply or current supply) from the power source (e.g. a battery). The processing continues by enabling functionality of the stand-alone integrated circuit when the at least one supply has substantially reached a steady state condition. With such a method and apparatus, a stand-alone integrated circuit may be properly enabled such that when the functional circuitry of a stand-alone integrated circuit is enabled it is enabled in a known state to ensure proper operation of the integrated circuit.

The present invention can be more fully described with reference to Figures 1 through 4. Figure 1 illustrates a schematic block diagram of a stand-alone integrated circuit 10 that includes a reset circuit 16, an on-chip power converter 18, functional circuitry 22, and a supply lock circuit 20. The stand-alone integrated circuit 10 is operably coupled to an external power source 12, which may be a battery, solar power generator, or other power source that produces a voltage that is not the proper voltage for powering at least a portion of the stand-alone integrated circuit 10. The stand-alone integrated circuit 10 is also operably coupled to an external crystal 14 that provides an oscillation to the reset circuit 16.

The reset circuit 16 includes a reset module 24, a clock lock module 26, and a clock generator 28. When the power source 12 and the crystal 14 are coupled to the stand-alone integrated circuit 10, the clock generator 28 produces a clock signal 32. The clock lock module 26 monitors the clock signal 32 to determine when it has reached a steady state condition. The clock signal 32 has reached a steady state condition typically when it is producing a clock signal at approximately 10% of the ideal frequency of the desired clock signal. Note that the reset circuit 16 will hold the power converter enable signal 31 in an inactive state until the clock lock signal 34 is asserted.

The reset module 24 holds the reset signal 30 low such that the functional circuitry 22 is held in an idle condition until the supply lock signal 44 is asserted as well as the clock lock signal 34. The function of circuitry 22 may be a microprocessor, digital signal processor, state machine, logic circuitry, analog circuitry, and/or any combination of electrical components to perform a desired electrical response given an electrical stimulus.

The on-chip power converter 18 includes a band-gap reference 36, switching transistors 38 and a regulation module 40. The on-chip power converter 18 remains inactive until a power enable signal is asserted. Once asserted, the band-gap reference 36 generates a reference voltage that is supplied to the regulation module 40. The regulation module 40 receives the clock signal 32 and generates control signals that are provided to the switching transistors 38. Based on the control signals, the switching transistors 38 produce a regulated supply 42. The supply lock signal 20 and the functional circuitry 22 receive the regulated supply 42. For a more detailed discussion of the on-chip power converter 18, refer to co-pending patent application having a docket number of SIG000010, entitled METHOD AND APPARATUS FOR REGULATING A DC OUTPUT VOLTAGE, having a Serial Number of 09/551,123, and a filing date of April 18, 2000.

The supply lock circuit 20 receives the supply 42 and determines when it has reached a steady state. The supply lock circuit 20 determines that the supply 42 reaches a steady state when the supply reaches at least 90% of its desired value. When this occurs, the supply lock circuit 20 generates a supply lock signal 44.

The reset module 24 receives the supply lock signal 44 and, if the clock lock signal 34 is enabled, the reset module 24 clears the reset signal 30 thus removing the functional circuitry 22 from the idle state. Once removed from the idle state, the functional circuitry 22 may perform its desired function(s). As one of average skill in the art will appreciate, multiple functional circuits may be included on the stand-alone integrated circuit where each functional circuit may be controlled by the reset circuit 16

or may each have its own corresponding reset circuit 16. The on-chip power converter 18 may produce multiple supply voltages for powering different types of functional circuitries. For example, analog circuitry may require a 5 volt supply while digital circuitry may require a 3 volt supply. As one of average skill in the art may further appreciate, the clock signal 32 may be delayed from generation until the power enable signal is activated as opposed to being generated upon application of power source 12.

Figure 2 illustrates a schematic block diagram of an alternate stand-alone integrated circuit 50. The stand-alone integrated circuit 50 includes the on-chip power converter 18, the functional circuitry 22, a processing module 52, and memory 54. The processing module 52 may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcomputer, digital signal processor, state machine, logic circuitry, and/or any device that manipulates signals (analog or digital) based on operational instructions. The memory 54 may be a single memory device or a plurality of memory devices. Such a memory device may be read only memory, random access memory, system memory, and/or any device that stores digital information. Note that when the processing module 52 implements one or more of its functions via a state machine or logic circuit, the memory storing the corresponding operational instruction is embedded within the circuitry comprising the state machine and/or logic circuit.

In general, the processing module 52 receives a power enable signal 56. Based on the power enable signal, the processing module performs a plurality of processing steps, which are discussed in greater detail with reference to Figure 3, to produce an enable signal 58. The enable signal 58 causes the on-chip power converter 18 to produce supply 42. Once the supply 42 reaches a steady state, the processing module 52 clears the reset signal 30 such that the functional circuit 22 may become active.

Figure 3 illustrates a logic diagram of a method for enabling a stand-alone integrated circuit. The process begins at Step 60 where an idle state is established. The idle state holds at least a portion of the stand-alone integrated circuit in a reset condition

when a power source is operably coupled to the stand-alone integrated circuit. For example, when a battery is coupled to the stand-alone integrated circuit the functional circuitry is held in an idle, or inactive state. The process then proceeds to Step 62 where a power enable signal is received. The process then proceeds to Step 64 where, in response to the power enable signal, an on-chip power converter of the stand-alone integrated circuit is enabled to generate at least one supply from the power source. The on-chip power converter may produce one or more supplies, which may be a voltage supply, or a current supply, for powering different functional circuits of the stand-alone integrated circuit. The process then proceeds to Step 56 where the functional circuitry of the stand-alone circuit is enabled when the at least one supply has substantially reached a steady state condition.

Processing Steps 64 and 66 may be described in further detail with reference to Steps 64-1 through 64-4 and Steps 66-1 through 66-3. At Step 64-1, a clock signal is generated. The processing then proceeds to Step 64-2 and Step 64-4. At Step 64-4, a clock lock signal is generated when the clock has substantially reached a steady state condition. At Step 64-2, power converter regulation signals are generated based on the clock signal. The process then proceeds to Step 64-3 where a band-gap reference is enabled. The band-gap reference is used to generate the power converter regulation signals. The process then proceeds to Step 66-1 where the clock lock signal is detected. The process then proceeds to Step 66-2 where a supply lock signal is detected. The process then proceeds to Step 66-3 where the reset signal is de-asserted upon detection of the clock lock signal and the power supply lock signal.

The processing of Step 60 may further be described with reference to Steps 60-A to Step 60-B and Step 66-A. At Step 60-A, a reset signal is enabled for at least a portion of the stand-alone integrated circuit. The portion of the stand-alone integrated circuit may be for a corresponding functional circuitry where each functional circuitry has its own reset signal or the reset signal may be applicable for the entire integrated circuit. The process then proceeds to Step 60- B where a clock signal is generated. The process

then proceeds to Step 66-A where the clock signal is provided to the components of the stand-alone integrated circuit and the reset signal is de-asserted.

Figure 4 illustrates a schematic block diagram of an embodiment of the reset circuit 16. The reset circuit 16 includes P-channel transistors 70 and 76, N-channel transistors 78 and 104, and logic elements 72, 80, 86, 88, 84, and 90. Also shown in Figure 4 are the regulation module 40, a transistor 92 of the switching transistors 38, and the clock lock module 26.

When the power source 12 is coupled to the stand-alone integrated circuit and the power enable, or power-up signal 94, has not been activated, resistor 82 holds the output of OR gate 80 low such that the power converter enable signal 31 is low. The regulation module 40 then pulls the gate of transistor 92 low, making the power source 12 substantially equal to the power supply 42. By enabling the power source to be coupled to the supply 42 in this manner, power can be provided to limited portions of the stand-alone integrated circuit including portions of the reset circuit 16 and the clock generator 28. With the power source connected to the stand-alone integrated circuit and the crystal 14 connected to the stand-alone integrated circuit, a crystal input 98 is provided to an input of a NAND gate 86 and to an input of the clock lock module 26. The other input of NAND gate 86 is received from the non-inverting output of D flip-flop 84. The output of NAND gate 86 is coupled to inverter 88 wherein the output of inverter 88 is the clock signal 32. The inverting output of D flip-flop 84 is coupled to inverter 90 wherein the output of inverter 90 corresponds to the power converter enable signal 31. The other input of the clock lock module 26 is the output of the logic gate 38. The output of the clock lock module 26 is connected to the RB and D inputs of the D-flip-flop 84.

When the power-up signal 94 is enabled, the output of OR gate 80 goes high thereby enabling the clock lock module 26. Once the output of the clock lock module 26 goes high, the power converter enable signal 31 is activated. This causes the regulation module 40 to provide a control signal to transistor 92 such that the supply 42 is generated at the desired output level. Once the supply has reached a steady state condition, the

converter lock signal 96 is generated thereby holding the output of OR gate 80 high. Note that the reset signal 30 could be generates as a signal equivalent to the converter lock signal 96 or as a logic AND of the converter lock signal 96 and the output of the clock lock module 26.

When the on-chip converter is turned off, the converter off signal 102 is activated high thereby enabling transistor 104. This actively pulls down on the output of logic gate 80 causing the clock lock module 26 to be disabled. This, in turn, resets the D flip-flop 84 and returns the regulation module 40 to a reset condition.

The preceding discussion has presented a method and apparatus for enabling a stand-alone integrated circuit. A stand-alone integrated circuit includes its own on-chip power converter such that an appropriate sequence of enabling the circuitry is performed to conserve power and to insure accurate startup of the integrated circuit. As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims or spirit of the invention.

CLAIMS

What is claimed is:

1. A method for enabling a stand-alone integrated circuit (IC), the method comprises the steps of:

a) establishing an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

b) receiving a power enable signal;

c) enabling, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source; and

d) when the at least one supply has substantially reached a steady-state condition, enabling functionality of the stand-alone IC.

2. The method of claim 1, wherein the establishing the idle state further comprises enabling a reset signal for the at least a portion of the stand-alone IC.

3. The method of claim 2, wherein the establishing the idle state further comprises generating a clock signal.

4. The method of claim 3, wherein the enabling of the functionality of the stand-alone IC further comprises providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

5. The method of claim 1, wherein the enabling the on-chip power converter further comprises:

generating a clock signal; and

generating power converter regulation signals based on the clock signal.

6. The method of claim 5, wherein the enabling the on-chip power converter further comprises enabling a band-gap reference that is used in generating the power converter regulation signals.

7. The method of claim 5 further comprises generating a clock lock signal when the clock has substantially reached a substantially steady-state.

8. The method of claim 7, wherein the enabling functionality of the stand-alone IC further comprises:

detecting the clock lock signal; and

detecting a supply lock signal; and

de-asserting a reset signal upon detection of the clock lock signal and the power supply lock signal.

9. The method of claim 1, wherein the enabling the on-chip converter further comprises:

generating a first supply from the power source; and

generating a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.

10. A stand-alone integrated circuit (IC) comprises:

a reset circuit operable to place the stand-alone IC in an idle state until a supply lock signal is enabled;

an on-chip power converter that generates a supply from an external power source upon assertion of a power enable signal; and

supply lock circuit operably coupled to enable the supply lock signal when the supply substantially reaches a steady-state condition.

11. The stand-alone IC of claim 10, wherein the reset circuit further comprises:

clock generator operably coupled to produce a clock signal when the external power source is coupled to the stand-alone IC, wherein the clock signal is provided to the on-chip power converter such that the on-chip power converter generates the supply;

clock lock module operably coupled to generate a clock lock signal when the clock signal has substantially reached a steady-state condition;

reset module operably coupled to assert a reset signal when the external power source is coupled to the stand-alone IC, wherein the reset module de-asserts the reset signal when the clock lock signal and the supply lock signal are asserted such that functionality of the stand-alone IC is enabled.

12. The stand-alone IC of claim 10, wherein the on-chip power converter further comprises:

a band-gap reference that produces a reference voltage upon assertion of the power enable signal.

13. The stand-alone IC of claim 10, wherein the on-chip power converter further comprises:

switching transistors operably coupled to produce a first supply and a second supply from the external power source and a single inductor, and

regulation module operably coupled to the switching transistors, wherein the regulation module produces control signals that enable and disable transistors of the switching transistors to regulate the first and second supplies.

14. A stand-alone IC comprises:

on-chip power converter;

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

establish an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC;

receive a power enable signal;

enable, in response to the power enable signal, the on-chip power converter of the stand-alone IC to generate at least one supply from the power source; and

when the at least one supply has substantially reached a steady-state condition, enable functionality of the stand-alone IC.

15. The stand-alone IC of claim 14, wherein the memory further comprises operational instructions that cause the processing module to establish the idle state by enabling a reset signal for the at least a portion of the stand-alone IC.

16. The method of claim 2, wherein the establishing the idle state further comprises generating a clock signal.

17. The stand-alone IC of claim 15, wherein the memory further comprises operational instructions that cause the processing module to enable the functionality of the stand-alone IC by providing the clock signal to components of the stand-alone IC and de-asserting the reset signal.

18. The stand-alone IC of claim 14, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip power converter by:

generating a clock signal; and

generating power converter regulation signals based on the clock signal.

19. The stand-alone IC of claim 18, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip power converter by enabling a band-gap reference that is used in generating the power converter regulation signals.

20. The stand-alone IC of claim 18, wherein the memory further comprises operational instructions that cause the processing module to generate a clock lock signal when the clock has substantially reached a substantially steady-state.

21. The stand-alone IC of claim 20, wherein the memory further comprises operational instructions that cause the processing module to enable functionality of the stand-alone IC further comprises:

detect the clock lock signal; and

detect a supply lock signal; and

de-assert a reset signal upon detection of the clock lock signal and the power supply lock signal.

22. The stand-alone IC of claim 14, wherein the memory further comprises operational instructions that cause the processing module to enable the on-chip converter further comprises:

generate a first supply from the power source; and

generate a second supply from the power source, wherein the first and second supplies are produced by regulating energy transfer from a single inductor.

METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

ABSTRACT OF THE DISCLOSURE

A method and apparatus for enabling a stand-alone integrated circuit (IC) includes processing that begins by establishing an idle state that holds at least a portion of the stand-alone integrated circuit in a reset condition when a power source is operably coupled to the stand-alone integrated circuit. A stand-alone integrated circuit includes generally an on-chip power converter, a reset circuit and some functional circuitry, which may be a microprocessor, digital signal processor, digital circuitry, state machine, logic circuitry, analog circuitry, and/or any type of components and/or circuits that perform a desired electrical function. When a power enable signal is received, the on-chip power converter is enabled to generate at least 1 supply from the power source. The processing continues by enabling functionality of the stand-alone integrated circuit when the at least one supply has substantially reached a steady state condition.

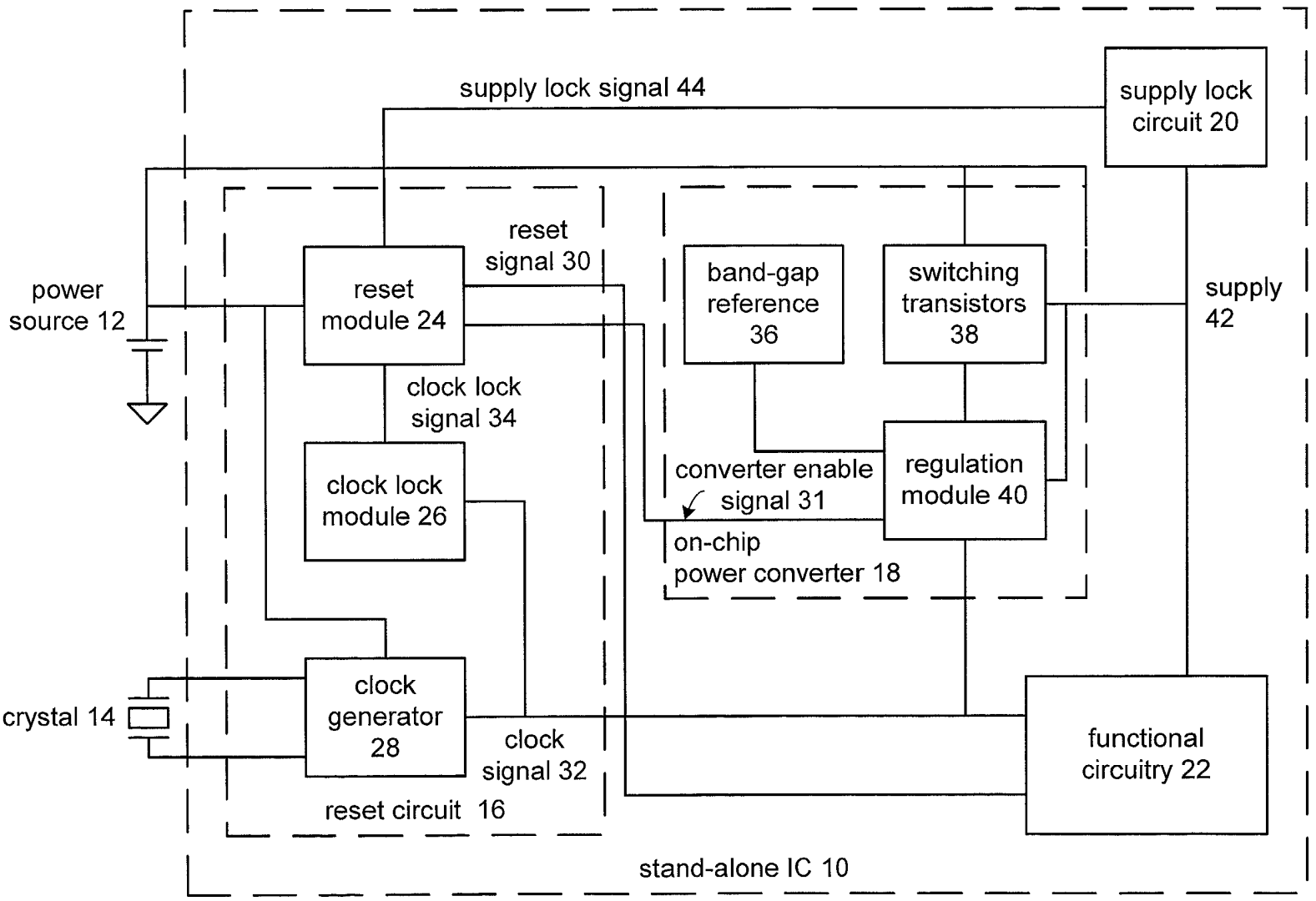
supply lock signal 44
supply lock circuit 20
reset signal 30
power source 12
reset module 24
band-gap reference 36
switching transistors 38
supply 42
clock lock signal 34
clock lock module 26
converter enable signal 31
regulation module 40
on-chip power converter 18
crystal 14
clock generator 28
clock signal 32
functional circuitry 22
reset circuit 16
stand-alone IC 10

FIG. 1

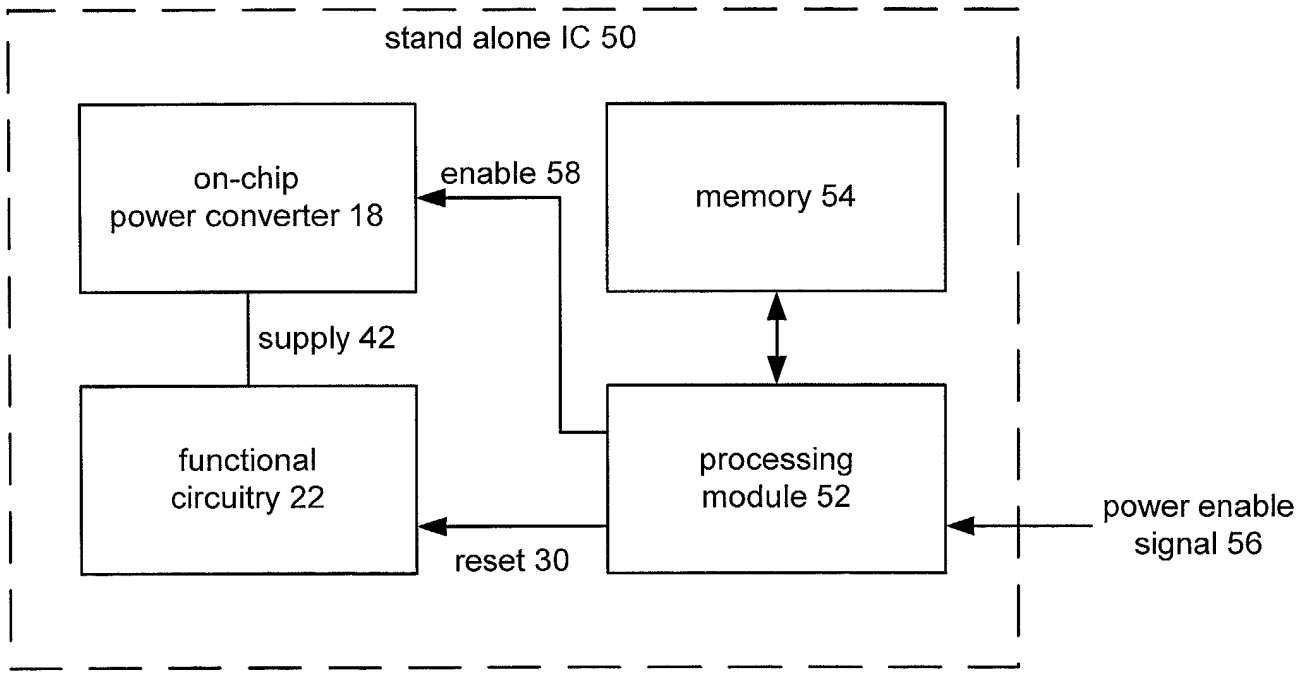
stand alone IC 50
on-chip
power converter 18
enable 58
memory 54
supply 42
functional
circuitry 22
processing
module 52
power enable
signal 56
reset 30

FIG. 2

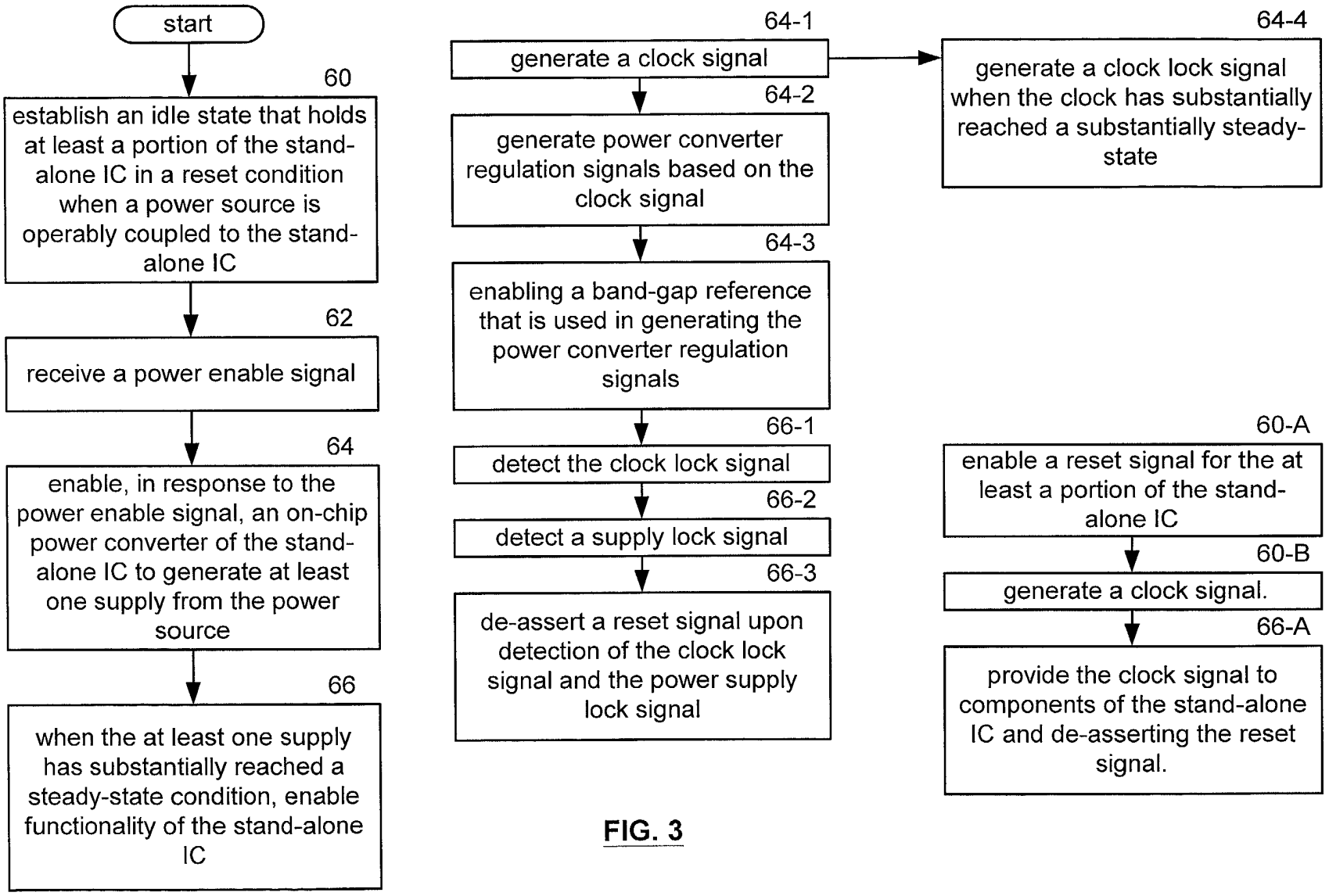
start
60
establish an idle state that holds at least a portion of the stand-alone IC in a reset condition when a power source is operably coupled to the stand-alone IC
62
receive a power enable signal
64
enable, in response to the power enable signal, an on-chip power converter of the stand-alone IC to generate at least one supply from the power source
66
when the at least one supply has substantially reached a steady-state condition, enable functionality of the stand-alone IC
64-1
generate a clock signal
64-2
generate power converter regulation signals based on the clock signal
64-3
enabling a band-gap reference that is used in generating the power converter regulation signals
66-1
detect the clock lock signal
66-2
detect a supply lock signal
66-3
de-assert a reset signal upon detection of the clock lock signal and the power supply lock signal
64-4
generate a clock lock signal when the clock has substantially reached a substantially steady-state
60-A
enable a reset signal for the at least a portion of the stand-alone IC
60-B
generate a clock signal.
66-A
provide the clock signal to components of the stand-alone IC and de-asserting the reset signal.

FIG. 3

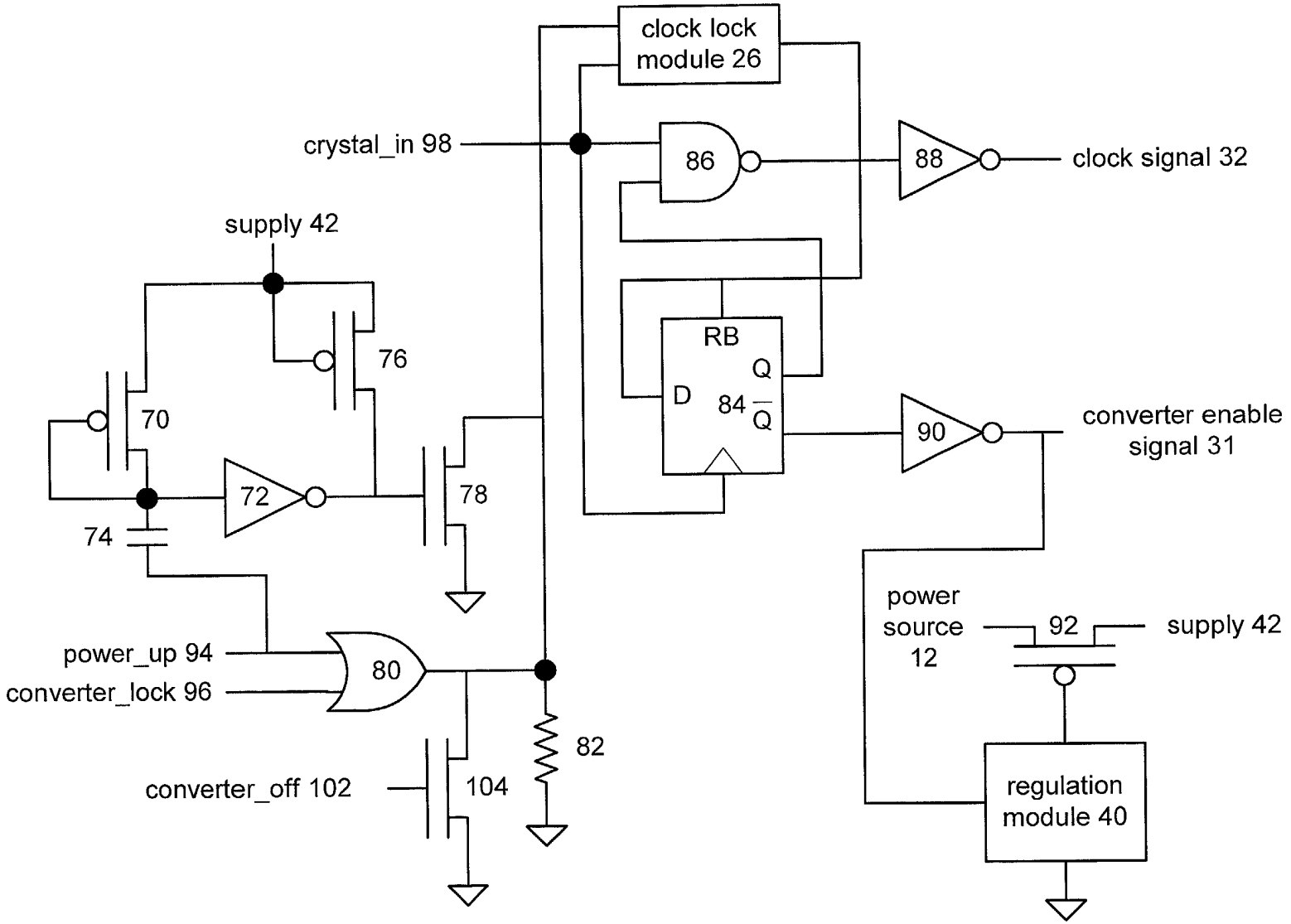
clock lock module 26
crystal_in 98
86
88
clock signal 32
supply 42
76
70
RB
Q
D
84
Q
converter enable signal 31
90
72
78
74
power source 12
92
supply 42
power_up 94
converter_lock 96
80
82
converter_off 102
104
regulation module 40

FIG. 4 16

PATENT APPLICATION
Docket No.: SIG000050

DECLARATION AND POWER OF ATTORNEY
Pursuant to 37 C.F.R 1.63 and 1.67

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name; and
I believe that I an inventor of the subject matter of a patent application entitled:

A METHOD AND APPARATUS FOR ENABLING A STAND ALONE INTEGRATED CIRCUIT

The specification for the patent application (check one):

[X] is attached hereto.

[ ] was filed on as Application Serial No.
and was amended on (if applicable).

[ ] was filed as PCT International Application No. PCT/ on
and was amended on (if applicable).

[ ] was filed on as Application Serial No.
and was issued a Notice of Allowance on

I hereby state that I have reviewed and understood the contents of the above identified patent application, including the claims as amended by any amendment referred to above or as allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this patent application as defined in 37 C.F.R. Section 1.56. If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 C.F.R. Section 1.56 which became available between the filing data of the prior application and the national or PCT international filing date of this CIP application.

I hereby claim foreign priority benefits under 35 U.S.C. Sections 119 and 365 of any foreign application(s) for patent(s) or inventor's certificate(s) listed below. I have also identified below any foreign application(s) for patent(s) or inventor's certificate(s) filed by me or my assignee which: disclose the subject matter claimed in this patent application; and have a filing date that is either (1) before the filing date of the application on which my priority is claimed; or, (2) before the filing date of this application when no priority is claimed:

Prior Foreign Patents
(list number, country, filing date MDY, date laid open, date granted or patented)

I hereby claim the benefit under 35 U.S.C. Sections 120 and 365 of any United States application(s) listed below and PCT international application(s) listed below:

Prior U.S. or PCT Applications

Application No.	Mo/Day/Yr Filed	Status

I hereby appoint Timothy W. Markison, Registration No. 33,534 of SigmaTel Inc., 2700 Via Fortuna, Sutie 500, Austin, Texas 78746 as my attorney, with full power of substitution and revocation, to prosecute this patent application and to transact all business in the United States Patent and Trademark Office connected therewith, and to file and prosecute any international patent applications filed thereon before any international authorities under the Patent Cooperation Treaty, and I hereby authorize him to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct them in writing to the contrary.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this patent application or any patent issued thereon.

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